that in Fig. 2 -- before "Fig. **4** is a schematic", and

change "Fig. **4** is a schematic" to --Fig. **5** is a schematic--;

and

line 12, change "Fig. **5**" to --Fig. **6**--.

IN THE CLAIMS:

Amend Claim 9 as follows:

1   19. (Once amended) A Miller-compensated amplifier, for amplifying

2   an input signal applied to an amplifier input node to provide an output

3   signal at an amplifier output node, comprising:

4   a first amplifier stage having an internal node as an input

5   thereto, and having a first stage output node;

6   a second amplifier stage having said amplifier input node as

7   an input thereto, and having a second stage output node;

8   a third amplifier stage having a third stage input node

9   coupled to said first stage output node and to said second stage

10   output node, and providing said output signal at said amplifier

11   output node; and

12   a capacitor coupled between said amplifier output node and

13   said internal node so as to provide voltage-mode gain.

Add the following new Claims 10 - 13:

1   2. 10.   A Miller-compensated amplifier according to Claim 1,

2   wherein said capacitor is connected such that a left-hand-plane zero is

3   provided in said compensated amplifier.

1 3 11. A compensated amplifier according to Claim 2 10, wherein said

2 left-hand-plane zero is selected so as to optimize compensation for said

3 compensated amplifier.

1 4 12. A compensated amplifier according to Claim 1 9, wherein said

2 first amplifier stage comprises a diode connected transistor and a ratioed

3 transistor connected together forming a current mirror, and wherein said

4 diode connected transistor senses said capacitive current at said internal

5 node and said ratioed transistor amplifies said capacitive current.

1 5 13. A Miller-compensated amplifier, for amplifying a differential

2 input signal applied to an amplifier input node to provide an output signal

3 at an amplifier output node, comprising:

4   a differential amplifier, for converting the voltage of said

5 differential input signal to differential input currents;

6   a bias voltage source;

7   a first FET and a second FET;

8   first and second current mirrors each mirroring one of said

9 differential input currents to one of said first and said second FETs,

10 said first current mirror comprising a third FET and a fourth FET

11 having a common gate connection node, and said second current

12 mirror comprising a fifth FET and a sixth FET having a common

13 gate connection node;

14   a third current mirror providing current to said first FET and

15 to said second FET;

16   a seventh FET sensing, at a gate thereof, a voltage on one of

17 said first FET and said second FET, and having a source thereof

18 connected to a voltage source;